

Hyunwoo Oh

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EDUCATION

M.S. in Electronic Engineering

2023

Seoul National University of Science and Technology (SEOULTECH)

Seoul, Korea

• Thesis: Research on Optimized Processor and Floating-point Unit Architecture for Embedded Systems

Supervisor: Seung Eun Lee

B.S. in Electronic Engineering

2021

Seoul National University of Science and Technology (SEOULTECH)

Seoul, Korea

SELECTED PUBLICATIONS (7 OUT OF 16) [\[SEE ALL ↓↓\]](#)

RF2P: A Lightweight RISC Processor Optimized for Rapid Migration from IEEE-754 to Posit.

Hyun Woo Oh, Seongmo An, Won Sik Jeong, Seung Eun Lee.

ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2023. [Oral Presentation] [\[Link\]](#) [\[Slides\]](#)

The Design of Optimized RISC Processor for Edge Artificial Intelligence Based on Custom Instruction Set Extension.

Hyun Woo Oh, Seung Eun Lee.

IEEE Access, Vol. 11, 2023. (SCIE, IF=3.9) [\[Link\]](#)

DL-Sort: A Hybrid Approach to Scalable Hardware-Accelerated Fully-Streaming Sorting.

Hyun Woo Oh, Jounghmin Park, Seung Eun Lee.

IEEE International Symposium on Circuits and Systems (ISCAS), 2024. [Accepted] [\[Program Page\]](#) [\[Preprint\]](#)

An SoC FPGA-based Integrated Real-time Image Processor for Uncooled Infrared Focal Plane Array.

Hyun Woo Oh, Cheol-Ho Choi, Jeong Woo Cha, Hyunmin Choi, Joon Hwan Han, Jung-Ho Shin.

Euromicro Conference on Digital System Design (DSD), 2023. [Long Presentation] [In Press] [\[Program Page\]](#)

The Design of a 2D Graphics Accelerator for Embedded Systems.

Hyun Woo Oh, Ji Kwang Kim, Gwan Beom Hwang, Seung Eun Lee.

Electronics, Vol. 10, No. 4, 2021. (SCIE, IF=2.9) [\[Link\]](#)

Lossless Decompression Accelerator for Embedded Processor with GUI.

Gwan Beom Hwang, Kwon Neung Cho, Chang Yeop Han, Hyun Woo Oh, Young Hyun Yoon, Seung Eun Lee.

Micromachines, Vol. 12, No. 2, 2021. (SCIE, IF=3.4) [\[Link\]](#)

ASimOV: A Framework for Simulation and Optimization of an Embedded AI Accelerator.

Dong Hyun Hwang, Chang Yeop Han, Hyun Woo Oh, Seung Eun Lee.

Micromachines, Vol. 12, No. 7, 2021. (SCIE, IF=3.4) [\[Link\]](#)

RESEARCH INTERESTS

I aim to explore scalable and sustainable solutions addressing evolving domain-specific computing demands. The key, I believe, lies in enhancing hardware scalability and integrating it with adequate software support to pick the positives of general-purpose processors (GPPs) and domain-specific architectures (DSAs): The abstractness of GPPs and the performance of DSAs.

- My research topics include but are not limited to:

Scalable HW/SW Co-Design: Exploring the co-optimization in scalable GPP/DSA-integrated architecture. This involves HW/SW architectural support and design space exploration to abstract complex hardware while optimizing resource use and performance.

CPU/DSA Configurability: Designing coarse-grained configurable architectures, adding novel abstracted scalable layers in logic- and microarchitecture-level. This involves hardwired schedulers, domain-specific accelerators, scalable ALUs, and custom instruction set extensions (ISEs).

Network Topologies: Investigating advanced network topologies for multi-core GPP/DSA architectures, focusing on enhancing communication efficiency and system performance in intricate computing environments.

RESEARCH EXPERIENCE

Research Assistant, SoC Platform Lab., SEOULTECH, Korea (Advisor: Prof. Seung Eun Lee)

Dec. 2019 - Feb. 2023

Posit Arithmetic HW/SW Architecture & Logic

- Designed a lightweight RISC processor supporting efficient IEEE-754 to Posit migration. [ISLPED 2023 (C6)] [ISOC2022 (C5)]
 - Challenge: ① Resource optimization for lightweight systems. ② IEEE-754 compatibility. ③ Testability.
 - Breakthrough: ① Scalable posit FPU (PAU) design. ② GCC compiler modification. ③ Rapid evaluation platform.
 - Result: ①-① Reduced area (11.00% and 57.87% fewer LUTs for PAU and divider, respectively) compared to state-of-the-art design. ①-② Reduced latency (Divide: 32 cycles → 13 cycles). ①-③ 60.09× throughput compared to SW (for approx. exponential function). ② SW Abstraction of Posit same as IEEE-754. ③ Verified through evaluation.

HW/SW Architecture of Scalable Embedded AI-Augmented General-Purpose Processor

- Designed a lightweight RISC core with architectural scalable k -NN acceleration support. [IEEE Access (J6)]
 - Challenge: ① Communication bottlenecks of separated GPP/DSA architecture. ② Scalability.
 - Breakthrough: ① Custom ISE coupled with computational kernel parallelism. ② Parameterized RTL generator.
 - Result: Achieved up to 193.88× throughput and 52.75× energy efficiency compared to the previous GPP/DSA architecture.

Domain-Specific Accelerators for Respiratory Medical Device

- Designed a 2D graphics accelerator optimized for graph visualization tasks in respiratory medical devices. [Electronics (J2)]
 - Challenge: ① Efficient 2D graphics processing for lightweight systems. ② Limited memory bandwidth
 - Breakthrough: ① RTL design of Bresenham's line algorithm and other features. ② Independent frame-buffer memory.
 - Result: ① Low area usage (5050 LUTs and 3087 FFs on FPGA, 75.4K gates on 180 nm CMOS process). ② Acceptable throughput (5550 lines per second @ 1024×768).
- Developed a SW stack for Lempel-Ziv 77 (LZ77) lossless decompression accelerator: ① Modeling LZ77 algorithm to design hardware. ② Developing a SW stack for data pre-processing and evaluation. [Micromachines (J1)]

Modularized Embedded AI Accelerator

- Developed an RTL generator for a reconfigurable embedded AI accelerator supporting k -NN and RBF-NN. [Micromachines (J3)]
- Researched SW applications of the AI accelerator module. [Micromachines (J4)] [ICCE 2021 (C2)] [JICCE (J5)] [ICFICE 2022 (C3)]

Baseline RISC Processor Architecture

- Designed a processor from scratch to provide a foundation for future research. [ISOC2020 (C1)]
 - RTL Designs: ① Pipelined MIPS core with predictive data forwarding. ② Direct-mapped \$I, \$D cache controller. ③ System bus.
 - Features: ① Partially-bypassed datapath. ② High-radix divider.
 - Performance: 1.86, 0.55 DMIPS/MHz (compiled with -O2, -Oo flag), and operating up to 100MHz in Xilinx Zynq-7000 FPGAs.

Other projects: Scalable Sorting Accelerator [ISCAS 2024 (C9)], Configurable JTAG TAP RTL generator, LIN Controller IP [ICCE 2022 (C4)].

Participated in designing several digital ASIC chips using Synopsys EDA tools. [See list JJ]

WORK EXPERIENCE

Junior Engineer (Full-time), Core H/W Team, Hanwha Systems, Korea

Jan. 2023 - present

- Designing SoC FPGA-based embedded thermal vision system. [DSD 2023 (C8)] [DSD 2023 (C7)] [IEEE Access (J7)]
 - Relevant Skills: Zynq Ultrascale+ MPSoC, AXI4-compliant accelerator IP design, FreeRTOS with AMP, PCB schematic design.
 - Research Keywords: Image processing HW design, Caching for HW acceleration, Infrared focal plane arrays.
- Developing RTOS for heterogeneous MPSoC-based embedded thermal imaging module.
 - Relevant Skills: VLIW/SIMD programming, Image processing, TI TDA3x SoC, TI Vision SDK, Peripheral drivers (CAN, I²C, Timer).

TEACHING EXPERIENCE

Teaching Assistant for “Computer Architecture”, SEOULTECH

Fall 2021

- Grading

Teaching Assistant for “Digital System Design”, SEOULTECH

Spring 2021

- Grading, preparation of lab lecture materials

TECHNICAL SKILLS

RTL Design	Hardware Description Language Simulation	Verilog, SystemVerilog, Chisel Verilator, ModelSim
Cell-Based ASIC Design	Synopsys EDA Tools Cadence EDA Tools	VCS (Simulation), Verdi (Analysis), Formality (Validation) Design Compiler (Synthesis), IC Compiler I/II (Layout) StarRCXT (Parasitic Extraction), PrimeTime (STA) Virtuoso Layout Suite* (Layout) Calibre DRC*/LVS* (Physical/Layout Verification)
FPGA-based Design	Xilinx FPGA Tools Intel FPGA Tools	Vivado, Vitis Quartus II/Prime, Nios II EDS
Computer Programming	Languages Version Control Operating System Development	C, C++, Python, Perl, MATLAB Git, SVN FreeRTOS, TI Vision SDK, PetaLinux
PCB Design	Cadence CAD Tools	OrCAD Capture* (Schematic), Allegro PCB Designer* (Artwork)
Miscellaneous	Document Tools Familiar OS	LaTeX, Obsidian (Markdown) Ubuntu, Windows 10 (with WSL), CentOS

* stands for beginner level.

AWARDS AND HONORS

Academic Scholarship, SEOULTECH

2021

Future Talent Scholarship to pursue a M.S., SEOULTECH

2021 - 2022

President of the Institute of Semiconductor Engineers Award, 21st Korea Semiconductor Design Contest

2020

PROFESSIONAL SERVICES

Reviewer, 3 times, *IEEE Access*

2023

TRAINING

ISO 26262:2018 Functional Safety Engineering Course: Automotive Foundation Level (FSE-AFL), DNV

2023.01.02-01.04

Design of High-speed Memory Interface, IDEC

2022.12.09

Cell-based Chip Design Flow for Samsung 28nm Process, IDEC

2021.11.01-11.05

[Synopsys] Block-level Auto P&R utilizing IC Compiler II, IDEC

2021.10.19-10.21

Cell-based Chip Design Flow, IDEC

2021.07.05-07.09

[Infineon] Automotive Semiconductor Expert Training - Basic Course, KSIA

2021.06.30-07.02

Cell-based Chip Design Flow, IDEC

2020.08.10-08.14

MILITARY SERVICE

Full-time Reserve Service

Oct. 2015 - Jul. 2017

Republic of Korea Army

Seoul, Korea

Peer-Reviewed Conference Papers

C9. **DL-Sort: A Hybrid Approach to Scalable Hardware-Accelerated Fully-Streaming Sorting.**

Hyun Woo Oh, Jounghmin Park, Seung Eun Lee.

IEEE International Symposium on Circuits and Systems (ISCAS), 2024. [Accepted] [[Program Page](#)] [[Preprint](#)]

C8. **An SoC FPGA-based Integrated Real-time Image Processor for Uncooled Infrared Focal Plane Array.**

Hyun Woo Oh, Cheol-Ho Choi, Jeong Woo Cha, Hyunmin Choi, Joon Hwan Han, Jung-Ho Shin.

Euromicro Conference on Digital System Design (DSD), 2023. [Long Presentation] [In Press] [[Program Page](#)]

C7. **Disparity Refinement Processor Architecture utilizing Horizontal and Vertical Characteristics for Stereo Vision Systems.**

Cheol-Ho Choi, **Hyun Woo Oh**.

Euromicro Conference on Digital System Design (DSD), 2023. [Long Presentation] [In Press] [[Program Page](#)]

C6. **RF2P: A Lightweight RISC Processor Optimized for Rapid Migration from IEEE-754 to Posit.**

Hyun Woo Oh, Seongmo An, Won Sik Jeong, Seung Eun Lee.

ACM/IEEE International Symposium on Low Power Electronics and Design (ISLPED), 2023. [Oral Presentation] [[Link](#)] [[Slides](#)]

C5. **Evaluation of Posit Arithmetic on Machine Learning based on Approximate Exponential Functions.**

Hyun Woo Oh, Won Sik Jeong, Seung Eun Lee.

International SoC Design Conference (ISOCC), 2022. [[Link](#)]

C4. **A Local Interconnect Network Controller for Resource-Constrained Automotive Devices.**

Kwonneung Cho, **Hyun Woo Oh**, Jeongeun Kim, Young Woo Jeong, Seung Eun Lee.

IEEE International Conference on Consumer Electronics (ICCE), 2022. [[Link](#)]

C3. **Intelligent Transportation System based on an Edge AI.**

Young Woo Jeong, **Hyun Woo Oh**, Su Yeon Jang, Seung Eun Lee.

International Conference on Future Information & Communication Engineering (ICFICE), 2022. [[Link](#)]

C2. **Vision-based Parking Occupation Detecting with Embedded AI Processor.**

Kwonneung Cho, **Hyun Woo Oh**, Seung Eun Lee.

IEEE International Conference on Consumer Electronics (ICCE), 2021. [[Link](#)]

C1. **Design of 32-bit Processor for Embedded Systems.**

Hyun Woo Oh, Kwon Neung Cho, Seung Eun Lee.

International SoC Design Conference (ISOCC), 2021. [[Link](#)]

Peer-Reviewed Journal Articles

J7. **Cell-Based Refinement Processor Utilizing Disparity Characteristics of Road Environment for SGM-based Stereo Vision Systems.**

Cheol-Ho Choi, **Hyun Woo Oh**, JoonHwan Han, Jungho Shin.

IEEE Access, Vol. 11, 2023. (SCIE, IF=3.9) [[Link](#)]

J6. **The Design of Optimized RISC Processor for Edge Artificial Intelligence Based on Custom Instruction Set Extension.**

Hyun Woo Oh, Seung Eun Lee.

IEEE Access, Vol. 11, 2023. (SCIE, IF=3.9) [[Link](#)]

J5. **An Edge AI Device based Intelligent Transportation System.**

Youngwoo Jeong, **Hyun Woo Oh**, Soohee Kim, Seung Eun Lee.

Journal of Information and Communication Convergence Engineering, Vol. 20, No. 3, 2022. (Scopus, CiteScore=1.1) [[Link](#)]

J4. **A Multi-Core Controller for an Embedded AI System Supporting Parallel Recognition.**

Suyeon Jang, **Hyun Woo Oh**, Young Hyun Yoon, Dong Hyun Hwang, Won Sik Jeong, Seung Eun Lee.

Micromachines, Vol. 12, No. 8, 2021. (SCIE, IF=3.4) [[Link](#)]

J3. **ASimOV: A Framework for Simulation and Optimization of an Embedded AI Accelerator.**

Dong Hyun Hwang, Chang Yeop Han, **Hyun Woo Oh**, Seung Eun Lee.

Micromachines, Vol. 12, No. 7, 2021. (SCIE, IF=3.4) [[Link](#)]

J2. The Design of a 2D Graphics Accelerator for Embedded Systems.

Hyun Woo Oh, Ji Kwang Kim, Gwan Beom Hwang, Seung Eun Lee.

Electronics, Vol. 10, No. 4, **2021**. (SCIE, IF=2.9) [\[Link\]](#)

J1. Lossless Decompression Accelerator for Embedded Processor with GUI.

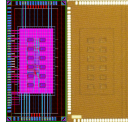
Gwan Beom Hwang, Kwon Neung Cho, Chang Yeop Han, **Hyun Woo Oh**, Young Hyun Yoon, Seung Eun Lee.

Micromachines, Vol. 12, No. 2, **2021**. (SCIE, IF=3.4) [\[Link\]](#)

CHIP DESIGNS [\[GO UP ↑\]](#)

A RISC-V Processor Supporting AMBA AXI Protocol for Embedded Systems

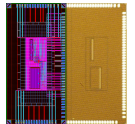
Jul. 2022



- Designer: Won Sik Jeong, Sun Beom Kwon, **Hyun Woo Oh**, Jeongeun Kim
- Technology: Samsung 28nm RFCMOS (1-poly 8-metal)
- Role: RTL Verification

Robot-Specific Processor for Autonomous Driving

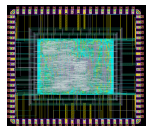
Jul. 2022



- Designer: Youngwoo Jeong, Yue Ri Jeong, **Hyun Woo Oh**, Kwang Hyun Go
- Technology: Samsung 28nm RFCMOS (1-poly 8-metal)
- Role: System Verification

In-Vehicle Network Processor based on Cortex-M0

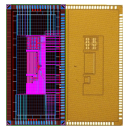
Mar. 2022



- Designer: Kwon Neung Cho, Jeong Eun Kim, **Hyun Woo Oh**
- Technology: TSMC 180nm RFCMOS (1-poly 6-metal)
- Role: System Verification SW Dev., RTL Verification, Pre/Post-Layout Simulation

A Programmable Embedded AI Processor with Cortex-M0

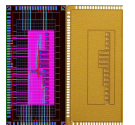
Jul. 2021



- Designer: Kwon Neung Cho, Young Woo Jeong, **Hyun Woo Oh**, Chang Yeop Han
- Technology: Samsung 28nm RFCMOS (1-poly 8-metal)
- Role: RTL Subblock Design

32-bit Processor with Posit Arithmetic Coprocessor for Embedded Systems

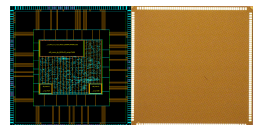
Jul. 2021



- Designer: **Hyun Woo Oh**, Jeong Eun Kim, Do Young Choi, Kwang Hyun Go
- Technology: Samsung 28nm RFCMOS (1-poly 8-metal)
- Role: RTL Design & Verification, ASIC Design Front-end/Back-end, Firmware, PCB Design & Chip Test

Implementation of Lossless Decompression Accelerator Based on Inflate Algorithm

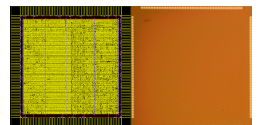
Sep. 2020



- Designer: Gwan Beom Hwang, Do Young Choi, **Hyun Woo Oh**, Chang Yeop Han
- Technology: Samsung 65nm RFCMOS (1-poly 8-metal)
- Role: System Verification SW Dev., PCB Design & Chip Test

Communication System with Simple and Fast Communication Error Check Code Based on CRC

Jun. 2020



- Designer: Chang Yeo Hanp, Kwon Neung Cho, **Hyun Woo Oh**
- Technology: Magnachip Hynix 0.18um CMOS
- Role: RTL Subblock Design