Hyunwoo Oh

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Education

Ph.D. Student in Computer Science **2024-present**
University of California, Irvine (UCI) Irvine, CA, USA
- Supervisor: Prof. Mohsen Imani

M.S. in Electronic Engineering **2021-2023**
Seoul National University of Science and Technology (SEOULTECH) Seoul, Korea
- Supervisor: Prof. Seung Eun Lee

B.S. in Electronic Engineering **2012-2021**
Seoul National University of Science and Technology (SEOULTECH) Seoul, Korea

Work Experiences

FPGA/Embedded SW Engineer (Full-time), Hanwha Systems, South Korea **Jan. 2023-Aug. 2024**

Selected Publications (4 out of 22) [See all ⇓]

DL-Sort: A Hybrid Approach to Scalable Hardware-Accelerated Fully-Streaming Sorting.
Hyun Woo Oh, Joungmin Park, Seung Eun Lee.
IEEE Transactions on Circuits and Systems II: Express Briefs (**TCAS-II**), vol. 71, no.5, **2024**.

RF2P: A Lightweight RISC Processor Optimized for Rapid Migration from IEEE-754 to Posit.
Hyun Woo Oh, Seongmo An, Won Sik Jeong, Seung Eun Lee.
*ACM/IEEE International Symposium on Low Power Electronics and Design (**ISLPED**)*, **2023**.

A Compact Real-Time Thermal Imaging System Based on Heterogeneous System-on-Chip.
Hyun Woo Oh, Cheol-Ho Choi, Jeong Woo Cha, Hyunmin Choi, Jung-Ho Shin, and Joon Hwan Han.
*IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (**RTCSA**)*, **2024**.

iTask: Task-Oriented Object Detection in Resource-Constrained Environments.
SungHeon Jeong, Hamza Errahmouni Barkam, **Hyunwoo Oh**, Hanning Chen, Tamoghno Das, Zhen Ye, and Mohsen Imani.
*ACM/IEEE Design Automation Conference (**DAC**)*, **2025**.

Professional Services

Technical Program Committee Member, *40th ACM/SIGAPP Symposium On Applied Computing (**SAC 2025**)* **2024-2025**
Reviewer, *IEEE Transactions on Circuits and Systems I: Regular Papers* **2024-**
Reviewer, *IEEE Access* **2023-**

Research/Industry Experiences

BIASLab, UCI (PI: Prof. Mohsen Imani) **Sep. 2024 - current**

ASIC Acceleration for ViT-NLP CLIP Model
- Designed a domain-specific accelerator for the ViT/NLP CLIP model for edge object detection. [DAC 2025 (C10)]

FPGA/Embedded SW Engineer (Full-time), Core H/W Team, Hanwha Systems, South Korea **Jan. 2023 - Aug. 2024**

- Designing SoC FPGA-based embedded thermal vision system. [DSD 2023 (C8)] [DSD 2023 (C7)] [IEEE Access (J7)]
  - Relevant Skills: Zynq Ultrascale+ MPSoC, AXI4-compliant accelerator IP design, FreeRTOS with AMP, PCB schematic design.
  - Research Keywords: Image processing HW design, Caching for HW acceleration, Infrared focal plane arrays.
- Developing RTOS for heterogeneous MPSoC-based embedded thermal imaging module. [RTCSA 2024 (C10)]
  - Relevant Skills: SIMD programming, VLIW, Image processing, TI TDA3x SoC, TI Vision SDK, Peripheral drivers (CAN, I^2C, Timer).

SoC Platform Lab., SEOULTECH, South Korea (PI: Prof. Seung Eun Lee) **Dec. 2019 - Feb. 2023**

Posit Arithmetic HW/SW Architecture
- Designed a lightweight RISC processor supporting efficient IEEE-754 to Posit migration. [ISLPED 2023 (C6)] [ISOCC 2022 (C5)]

HW/SW Architecture of Scalable Embedded AI-Augmented General-Purpose Processor
- Designed a lightweight RISC core with architectural scalable *k*-NN acceleration support. [IEEE Access (J6)]

Domain-Specific Accelerators for Respiratory Medical Device
- Designed a 2D graphics accelerator optimized for graph visualization tasks in respiratory medical devices. [Electronics (J2)]

- Developed a SW stack for Lempel-Ziv 77 (LZ77) lossless decompression accelerator: ① Modeling LZ77 algorithm to design hardware. ② Developing a SW stack for data pre-processing and evaluation. [Micromachines (J1)]

Modularized Embedded AI Accelerator
- Developed an RTL generator for a reconfigurable embedded AI accelerator supporting *k*-NN and RBF-NN. [Micromachines (J3)]
- Researched SW applications of the AI accelerator module. [Micromachines (J4)] [ICCE 2021 (C2)] [JICCE (J5)] [ICFICE 2022 (C3)]

Baseline RISC Processor Architecture
- Designed a processor from scratch to provide a foundation for future research. [ISOCC 2020 (C1)]

Other projects: Scalable Sorting Accelerator [TCAS-II (J8)], Configurable JTAG TAP RTL generator, LIN Controller IP [ICCE 2022 (C4)].

Participated in several ASIC design projects using Synopsys EDA tools. [See list ⇓]

Teaching Experience

Teaching Assistant for "Computer Architecture", SEOULTECH **Fall 2021**
Teaching Assistant for "Digital System Design", SEOULTECH **Spring 2021**

Awards and Honors

Computer Science Department Research Fellowship	University of California, Irvine	$ 18.7K	**2024**
Discretionary Merit Award	University of California, Irvine	$ 2.5K	**2024**
Future Talent Scholarship	Seoul National University of Science and Technology	$ 5.5K	**2021-2022**
Academic Scholarship	Seoul National University of Science and Technology	$ 0.4K	**2021**
President of the Institute of Semiconductor Engineers Award	21st Korea Semiconductor Design Contest	$ 0.9K	**2020**

Technical Skills

RTL Design	HDL	Verilog, SystemVerilog, Chisel
	Simulation	Verilator, ModelSim
Cell-Based ASIC Design	Synopsys EDA Tools	Design Compiler (Synthesis), IC Compiler I/II (Layout)
		VCS (Simulation), Verdi (Analysis), Formality (Validation)
		StarRCXT (Parasitic Extraction), PrimeTime (STA)
	Cadence EDA Tools	Virtuoso Layout Suite (Layout), Calibre DRC/LVS (Physical/Layout Verification)
FPGA Design	Xilinx FPGA Tools	Vivado, Vitis
	Intel FPGA Tools	Quartus II/Prime, Nios II EDS
Computer Programming	Languages	C, C++, Python, MATLAB
	OS Development	FreeRTOS, TI Vision SDK, PetaLinux

Training

Design of High-speed Memory Interface, IDEC	**2022.12.09**
Cell-based Chip Design Flow for Samsung 28nm Process, IDEC	**2021.11.01-11.05**
[Synopsys] Block-level Auto P&R utilizing IC Compiler II, IDEC	**2021.10.19-10.21**
Cell-based Chip Design Flow, IDEC	**2021.07.05-07.09**
[Infineon] Automotive Semiconductor Expert Training - Basic Course, KSIA	**2021.06.30-07.02**
Cell-based Chip Design Flow, IDEC	**2020.08.10-08.14**

All Publications [Go up ⇑]

Conference Papers

C12. **iTask: Task-Oriented Object Detection in Resource-Constrained Environments**.
SungHeon Jeong, Hamza Errahmouni Barkam, **Hyunwoo Oh**, Hanning Chen, Tamoghno Das, Zhen Ye, and Mohsen Imani.
*ACM/IEEE Design Automation Conference (**DAC**)*, **2025**.

C11. **Algorithm for LWIR Thermal Imaging Camera with Minimal Mechanical Shutter Utilization**.
Taehyun Kim, Joonhwan Han, Jeongwoo Cha, Hyunmin Choi, Jungho Shin, Eunchong Kim, **Hyun Woo Oh**, *et al.*
IEEE International Conference on Consumer Electronics-Asia (**ICCE-Asia**), **2024**.

C10. **A Compact Real-Time Thermal Imaging System Based on Heterogeneous System-on-Chip**.
Hyun Woo Oh, Cheol-Ho Choi, Jeong Woo Cha, Hyunmin Choi, Jung-Ho Shin, and Joon Hwan Han.
*IEEE International Conference on Embedded and Real-Time Computing Systems and Applications (**RTCSA**)*, **2024**.

C9. **Fast Object Detection Algorithm using Edge-based Operation Skip Scheme with Viola-Jones Method**.
Cheol-Ho Choi, Joonhwan Han, Jeongwoo Cha, Jungho Shin, and **Hyun Woo Oh**.
*IEEE International Conference on Artificial Intelligence Circuits and Systems (**AICAS**)*, **2024**.

C8. **An SoC FPGA-based Integrated Real-time Image Processor for Uncooled Infrared Focal Plane Array**.
Hyun Woo Oh, Cheol-Ho Choi, Jeong Woo Cha, Hyunmin Choi, Joon Hwan Han, Jung-Ho Shin.
*Euromicro Conference on Digital System Design (**DSD**)*, **2023**.

C7. **Disparity Refinement Processor Architecture utilizing Horizontal and Vertical Characteristics for Stereo Vision Systems**.
Cheol-Ho Choi, **Hyun Woo Oh**.
*Euromicro Conference on Digital System Design (**DSD**)*, **2023**.

C6. **RF2P: A Lightweight RISC Processor Optimized for Rapid Migration from IEEE-754 to Posit**.
Hyun Woo Oh, Seongmo An, Won Sik Jeong, Seung Eun Lee.
*ACM/IEEE International Symposium on Low Power Electronics and Design (**ISLPED**)*, **2023**.

C5. **Evaluation of Posit Arithmetic on Machine Learning based on Approximate Exponential Functions**.
Hyun Woo Oh, Won Sik Jeong, Seung Eun Lee.
*International SoC Design Conference (**ISOCC**)*, **2022**.

C4. **A Local Interconnect Network Controller for Resource-Constrained Automotive Devices**.
Kwonneung Cho, **Hyun Woo Oh**, Jeongeun Kim, Young Woo Jeong, Seung Eun Lee.
*IEEE International Conference on Consumer Electronics (**ICCE**)*, **2022**.

C3. **Intelligent Transportation System based on an Edge AI**.
Young Woo Jeong, **Hyun Woo Oh**, Su Yeon Jang, Seung Eun Lee.
*International Conference on Future Information & Communication Engineering (**ICFICE**)*, **2022**.

C2. **Vision-based Parking Occupation Detecting with Embedded AI Processor**.
Kwonneung Cho, **Hyun Woo Oh**, Seung Eun Lee.
*IEEE International Conference on Consumer Electronics (**ICCE**)*, **2021**.

C1. **Design of 32-bit Processor for Embedded Systems**.
Hyun Woo Oh, Kwon Neung Cho, Seung Eun Lee.
*International SoC Design Conference (**ISOCC**)*, **2021**.

Journal Articles

J10. **EOS: Edge-Based Operation Skip Scheme for Real-Time Object Detection Using Viola-Jones Classifier**.
Cheol-Ho Choi, Joonhwan Han, **Hyun Woo Oh**, Jeongwoo Cha, and Jungho Shin.
Sensors, Vol. 24, No. 12, **2024**.

J9. **Contrast Enhancement Method using Region-based Dynamic Clipping Technique for LWIR-based Thermal Camera of Night Vision Systems**.
Cheol-Ho Choi, Joonhwan Han, Jeongwoo Cha, Hyunmin Choi, Jungho Shin, Taehyun Kim, and **Hyun Woo Oh**.
Sensors, Vol. 24, No. 12, **2024**.

J8. **DL-Sort: A Hybrid Approach to Scalable Hardware-Accelerated Fully-Streaming Sorting**.
Hyun Woo Oh, Joungmin Park, Seung Eun Lee.
IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 71, no.5, **2024**.

J7. **Cell-Based Refinement Processor Utilizing Disparity Characteristics of Road Environment for SGM-based Stereo Vision Systems**.
Cheol-Ho Choi, **Hyun Woo Oh**, JoonHwan Han, Jungho Shin.
IEEE Access, vol. 11, **2023**.

J6. **The Design of Optimized RISC Processor for Edge Artificial Intelligence Based on Custom Instruction Set Extension**.
Hyun Woo Oh, Seung Eun Lee.
IEEE Access, Vol. 11, **2023**.

J5. **An Edge AI Device based Intelligent Transportation System**.
Youngwoo Jeong, **Hyun Woo Oh**, Soohee Kim, Seung Eun Lee.
Journal of Information and Communication Convergence Engineering, Vol. 20, No. 3, **2022**.

J4. **A Multi-Core Controller for an Embedded AI System Supporting Parallel Recognition**.
Suyeon Jang, **Hyun Woo Oh**, Young Hyun Yoon, Dong Hyun Hwang, Won Sik Jeong, Seung Eun Lee.
Micromachines, Vol. 12, No. 8, **2021**.

J3. **ASimOV: A Framework for Simulation and Optimization of an Embedded AI Accelerator**.
Dong Hyun Hwang, Chang Yeop Han, **Hyun Woo Oh**, Seung Eun Lee.
Micromachines, Vol. 12, No. 7, **2021**.

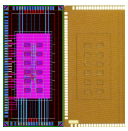
J2. **The Design of a 2D Graphics Accelerator for Embedded Systems**.
Hyun Woo Oh, Ji Kwang Kim, Gwan Beom Hwang, Seung Eun Lee.
Electronics, Vol. 10, No. 4, **2021**.

J1. **Lossless Decompression Accelerator for Embedded Processor with GUI**.
Gwan Beom Hwang, Kwon Neung Cho, Chang Yeop Han, **Hyun Woo Oh**, Young Hyun Yoon, Seung Eun Lee.
Micromachines, Vol. 12, No. 2, **2021**.

Chip Designs [Go up ⇑]

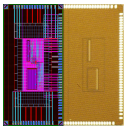
A RISC-V Processor Supporting AMBA AXI Protocol for Embedded Systems **Jul. 2022**

- Designer: Won Sik Jeong, Sun Beom Kwon, **Hyun Woo Oh**, Jeongeun Kim
- Technology: Samsung 28nm RFCMOS (1-poly 8-metal)
- Role: RTL Verification



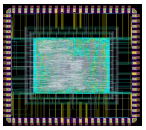
Robot-Specific Processor for Autonomous Driving **Jul. 2022**

- Designer: Youngwoo Jeong, Yue Ri Jeong, **Hyun Woo Oh**, Kwang Hyun Go
- Technology: Samsung 28nm RFCMOS (1-poly 8-metal)
- Role: System Verification



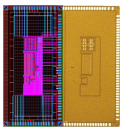
In-Vehicle Network Processor based on Cortex-M0 **Mar. 2022**

- Designer: Kwon Neung Cho, Jeong Eun Kim, **Hyun Woo Oh**
- Technology: TSMC 180nm RFCMOS (1-poly 6-metal)
- Role: System Verification SW Dev., RTL Verification, Pre/Post-Layout Simulation



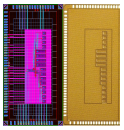
A Programmable Embedded AI Processor with Cortex-M0 **Jul. 2021**

- Designer: Kwon Neung Cho, Young Woo Jeong, **Hyun Woo Oh**, Chang Yeop Han
- Technology: Samsung 28nm RFCMOS (1-poly 8-metal)
- Role: RTL Subblock Design



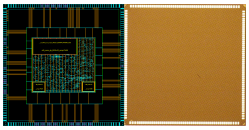
32-bit Processor with Posit Arithmetic Coprocessor for Embedded Systems **Jul. 2021**

- Designer: **Hyun Woo Oh**, Jeong Eun Kim, Do Young Choi, Kwang Hyun Go
- Technology: Samsung 28nm RFCMOS (1-poly 8-metal)
- Role: RTL Design & Verification, ASIC Design Front-end/Back-end, Firmware, PCB Design & Chip Test



Implementation of Lossless Decompression Accelerator Based on Inflate Algorithm **Sep. 2020**

- Designer: Gwan Beom Hwang, Do Young Choi, **Hyun Woo Oh**, Chang Yeop Han
- Technology: Samsung 65nm RFCMOS (1-poly 8-metal)
- Role: System Verification SW Dev., PCB Design & Chip Test



Communication System with Simple and Fast Communication Error Check Code Based on CRC **Jun. 2020**

- Designer: Chang Yeo Hanp, Kwon Neung Cho, **Hyun Woo Oh**
- Technology: Magnachip Hynix 0.18um CMOS
- Role: RTL Subblock Design