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Design of 32-bit Processor for Embedded Systems

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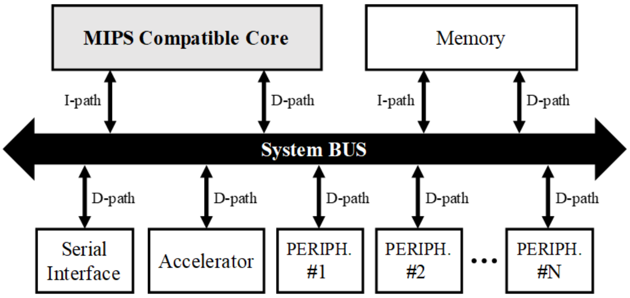
Abstract

In this paper, we propose a 32-bit processor for the embedded system. In order to provide less area and low power operation, we adopt MIPS instruction set architecture (ISA) to our processor. The processor consists of five pipeline stages to reduce the critical path. In order to solve the data hazard in pipeline stages, we design the data forwarding unit and stall unit with optimized bubble insertion. The processor is implemented on a field programmable gate array (FPGA), and we verify the functionality of the processor and measure the performance by using the Dhrystone benchmark. The Dhrystone MIPS (DMIPS) is measured at 27.71 at 50 MHz operation.

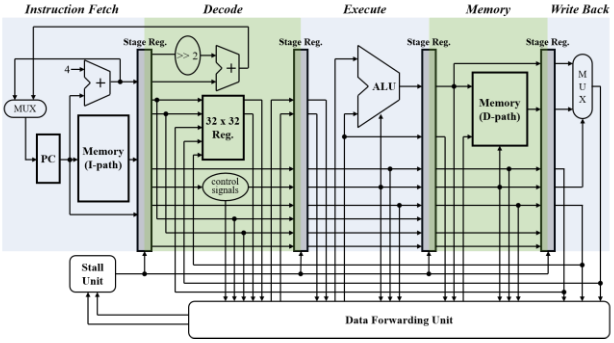
System Architecture

Our proposed system consists of **MIPS I ISA compatible core**, system bus, memory, and peripherals such as serial interface and accelerator. All the components of the processor are connected through the system bus, which contains the instruction path (I-path) and data path (D-path) to avoid the structural hazards by reading the instruction codes and data separately. The serial interface is included to provide communication with external devices.

The core includes the 32 of 32-bit GPRs, five pipeline stages, data forwarding unit, and stall unit. Each pipeline stage has a register that stores operands, addresses of operands, and control signals to execute.



[Entire architecture of the proposed processor]



[Block diagram of the MIPS core]

Data Forwarding & Stall

The data forwarding unit detects the data hazard by comparing the addresses for reading the GPRs in each current stage and the addresses for storing the data to the GPR in each next stage.

In addition, the data forwarding unit checks the write enable signal for the GPR in each stage to prevent forwarding the data that not to be written to the GPR. The data hazards are detected only when the write enable signal of each stage is set.

The data forwarding unit forwards the data from the closest hazard-detected stages to the current stage to deal with the data hazards when the data are able to be forwarded. On condition that the data hazard occurs but the data is unable to be forwarded, the data forwarding unit generates the **stall unit** control signal.

Implementation

We verify the functionality of our processor through the FPGA implementation and measure the performance of the processor by running the Dhrystone 2.1 benchmark. In order to check the execution time of the Dhrystone benchmark, we add the clock counter to the system bus.

The result shows that the performance and area usage of the processor is suitable for the embedded system.

TABLE I. DHRYSTONE BENCHMARK RESULT

Entity	Value
Run Count	131,072
Total Execution Time (in seconds)	2.69
Dhrystones per Second	48,685.48
Dhrystone VAX MIPS (DMIPS)	27.71
DMIPS / MHz	0.554

Compiled with mips-elf-gcc-5.3.0 and binutils-2.34

TABLE II. DEVICE UTILIZATION SUMMARY

Entity	Resource Usage
Total Logic Elements	6,032 / 24,624 (24 %)
4-input LUTs	3,439
3-input LUTs	1,406
<=2-input LUTs	860
Register only	327

Implemented on Altera Cyclone III EP3C25Q240 FPGA

Conclusion

In this paper, we proposed the 32-bit processor for the embedded system compatible with MIPS ISA. We implemented the processor on FPGA and the processor is verified and measured by using the Dhrystone benchmark. In the future work, we are planning to attach various accelerators to the processor. We expect that our processor is suitable for a variety of embedded systems.

Acknowledgment

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